SEMICONDUCTOR DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation application of International Application PCT/JP2014/072811, filed on Aug. 29, 2014, which claims its priority under Article 8 of the Patent Cooperation Treaty based on Japanese Patent Application No. 2013-194834, filed on Sep. 20, 2013, Japanese Patent Application No. 2014-148356, fined on Jul. 18, 2014, Japanese utility model registration application No. 2014-003865, filed on Jul. 7 18, 2014, and Japanese Patent Application No. 2014-155442, filed on Jul. 30, 2014, the entire contents of which are hereby incorporated by reference.

BACKGROUND

[0002] This disclosure relates to structures of trench gate type semiconductor devices performing switching operation.

[0003] Insulated gate bipolar transistors (IGBTs) having high input impedance and low on-voltage are used in motor driving circuits. The IGBTs, however, have a trade-off relation between breakdown voltage and on-voltage.

[0004] For such features of the IGBTs, a variety of approaches have been proposed to reduce the on-voltage while keeping the breakdown voltage high. For example, a structure has been proposed in which an n-type layer having a high impurity concentration than that of a drift region and configured to accumulate holes (hereinafter referred to as "carrier accumulation layer") is arranged between abase region and the drift region. Such a structure can prevent holes from a collector region from reaching an emitter electrode, thereby decreasing the on-voltage (for example, see Japanese Patent Application Publication No. 2002-353456 (PTL 1)).

SUMMARY

[0005] One aspect according to an embodiment provides a semiconductor device including (A) a first semiconductor region of a first conductivity type, (B) a second semiconductor region of a second conductivity type arranged on the first semiconductor region, (C) a third semiconductor region of the first conductivity type arranged on the second semiconductor region, (D) fourth semiconductor regions of the second conductivity type arranged on the third semiconductor region, (E) an insulation film arranged on an inner wall of a groove extending from the top surface of the fourth semiconductor region and reaching the second semiconductor region through the fourth semiconductor region and the third semiconductor region, (F) a control electrode arranged on a region of the insulation film at a side surface of the groove where the insulation film faces the third semiconductor region, (G) a first main electrode electrically connected to the first semiconductor region, (H) a second main electrode electrically connected to the fourth semiconductor region, and (I) a bottom electrode arranged on the insulation film at the bottom surface of the groove and spaced from the control electrode, the bottom electrode electrically connected to the second main electrode, wherein in plan view, the length of the groove in an extending direction thereof is equal to or more than the width of the groove, and the width of the groove is larger than the gap between the groove and an adjacent groove.

[0006] Another embodiment provides a semiconductor device including (A) first semiconductor region of a first conductivity type, (B) a second semiconductor region of a second conductivity type arranged on the first semiconductor region, (C) a third semiconductor region of the first conductivity type arranged on the second semiconductor region, (D) fourth semiconductor regions of the second conductivity type arranged on the third semiconductor region, (E) an insulation film arranged on an inner wall of groove extending from the top surface of the fourth semiconductor region and reaching the second semiconductor region through the fourth semiconductor region and the third semiconductor region, (F) a control electrode arranged on a region of the insulation film at a side surface of the groove where the insulation film faces the third semiconductor region, (G) a bottom electrode arranged on the insulation film and spaced from the control electrode on the bottom surface of the groove, (H) a first main electrode electrically connected to the first semiconductor region, (I) an interlayer insulation film arranged on the control electrode and the bottom electrode, and (J) a second main electrode arranged on the interlayer insulation film arranged on the third semiconductor region and on the fourth semiconductor regions and above the control electrode and the bottom electrode with the interlayer insulation film interposed in between, the second main electrode electrically connecting the fourth semiconductor region to the bottom electrode, wherein in plan view, the area of the groove is larger than the area of the semiconductor region between the groove and an adjacent groove.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. **1** is a schematic sectional view illustrating the structure of a semiconductor device according to one embodiment.

[0008] FIG. **2** is a graph illustrating the relationship between the width of a groove, the collector-emitter voltage, and the collector-emitter saturation voltage of the semiconductor device according to one embodiment.

[0009] FIGS. **3**A and **3**B illustrate the results of simulation of holes accumulated in a semiconductor device.

[0010] FIGS. **4**A and **4**B illustrate the results of simulation of potential distribution around the groove.

[0011] FIG. **5** is another graph illustrating the relationship between the width of the groove, the collector-emitter voltage, and the collector-emitter saturation voltage of a semiconductor device according to one embodiment.

[0012] FIGS. **6**A to **6**H are sectional views illustrating steps in a method of manufacturing a semiconductor device according to one embodiment.

[0013] FIGS. **7**I to **7**N are sectional views illustrating steps in the method of manufacturing a semiconductor device according to one embodiment (continued).

[0014] FIGS. **8**A and **8**B are schematic views illustrating the arrangement of a gate electrode, a bottom electrode, an insulation film, and an emitter region in the semiconductor device according to one embodiment; FIG. **8**A is a plan view, and FIG. **8**B is a sectional view taken along the VIII-VIII direction in FIG. **8**A.

[0015] FIG. **9** is a schematic perspective view illustrating an exemplary arrangement of an emitter region in the semiconductor device according to one embodiment.

[0016] FIG. **10** is a schematic perspective view illustrating another exemplary arrangement of the emitter region in the semiconductor device according to one embodiment.

[0017] FIG. **11** is a schematic plan view illustrating an exemplary arrangement of a groove and a connection groove in the semiconductor device according to one embodiment.